Addendum: Addition of timer relay on Unidrive SP size 6 and 7 free standing

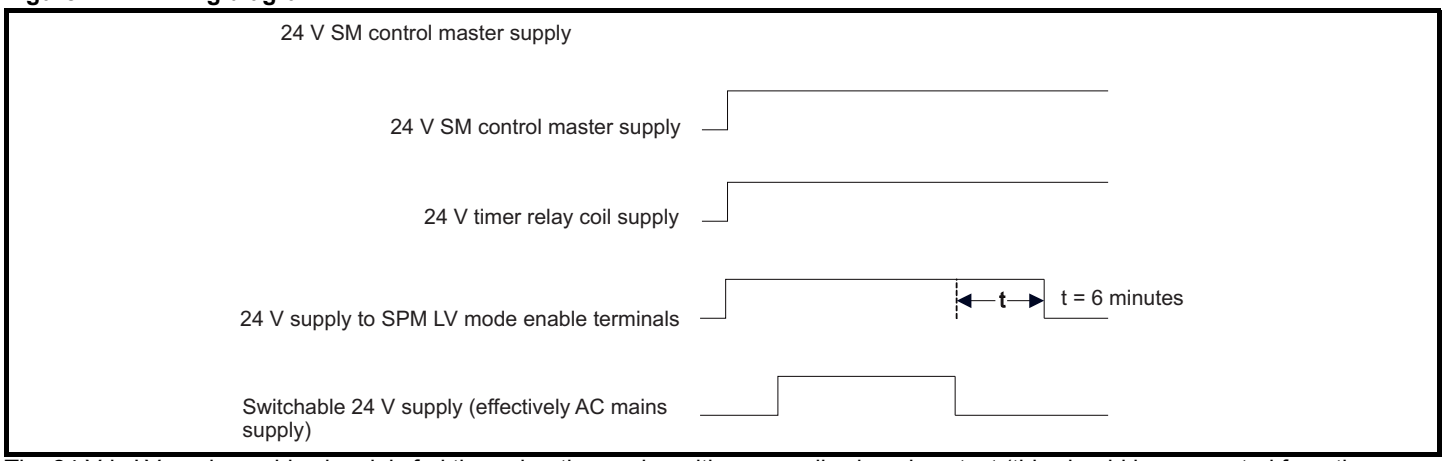
This addendum covers the introduction of a timer relay on Unidrive SP sizes 6 and 7 free standing units.

When initially supplying the control master pod with 24 Vdc and no mains supply to the power stage the control pod will display the 'inh' (inhibit status).

Where a UV condition is preferred (when initially supplying the control pod with an auxiliary 24 Vdc supply), the additional user connections and instructions outlined within this addendum should be implemented. This is achieved by controlling a 24 Vdc supply to the SPM inverter low voltage DC mode enable terminals using a timer relay.

Establishing the user connections outlined in wiring diagrams Figure 1-3 *Unidrive SP6 wiring diagram* and Figure 1-4 *Unidrive SP7 wiring diagram* including connecting an external 24 Vdc signal to the normally closed contacts of the timer relay, will ensure that the control pod displays the UV condition when initially supplied by 24 Vdc only. When the high voltage mains supply is applied the LV DC mode enable signal will be removed, and when the mains supply is removed a delay of 6 minutes is applied before the LV mode enable signal is reapplied to prevent a LV mode over voltage trip or 'inh' status (with the latter present for a short period when the DC bus is greater than 35 V but less than the LV mode over voltage threshold) as illustrated in Figure 1-1.

Figure 1-1 Timing diagram

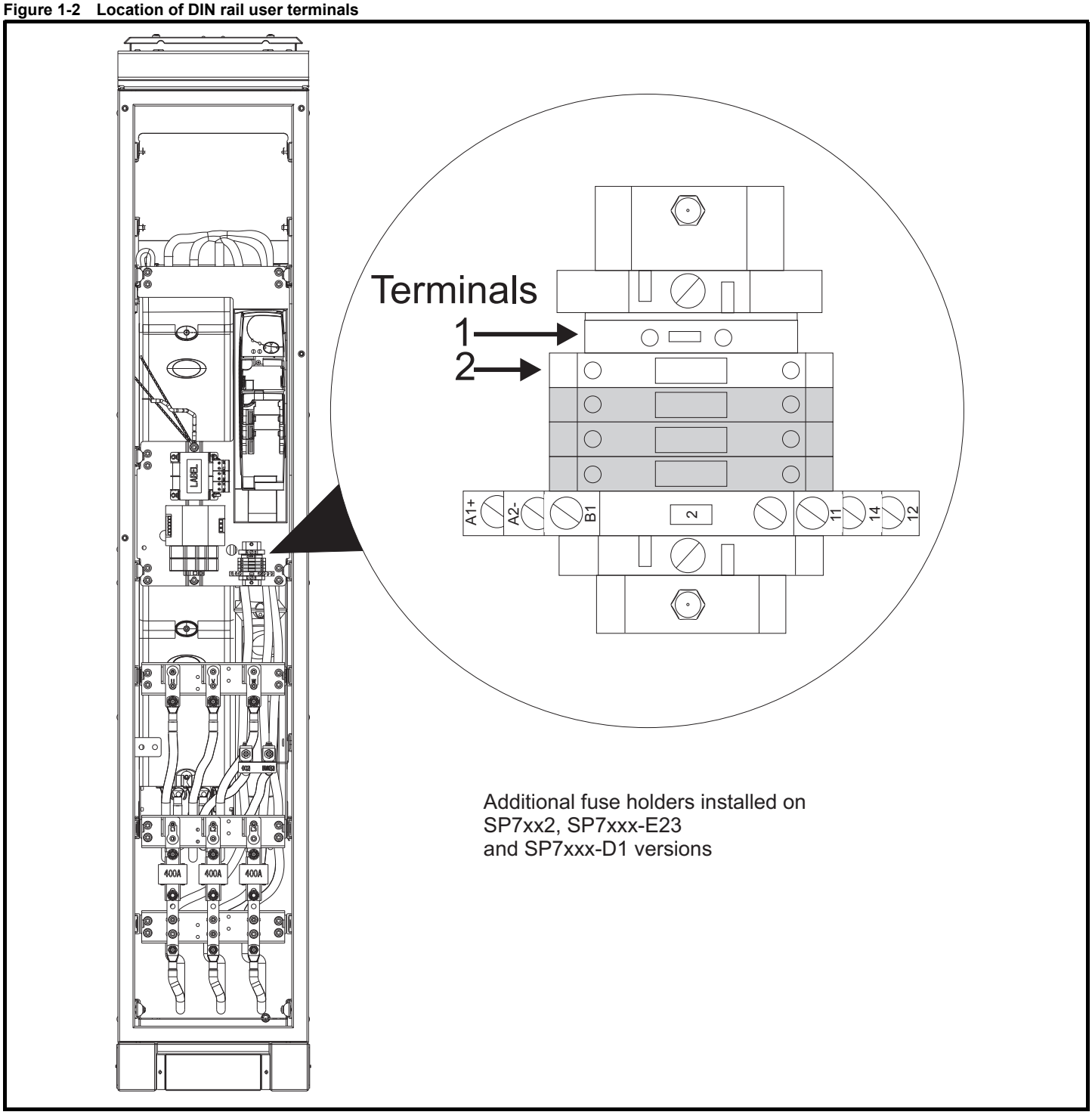


The 24 Vdc LV mode enable signal, is fed through a timer relay with a normally closed contact (this should be generated from the same external supply as the SM control master auxiliary 24 Vdc and timer relay coil). The internal SMPS 24 Vdc output is connected to the control contact on the relay when the AC supply is removed, the relay contact is held in the open condition for 6 minutes (delay off) to prevent a low voltage mode 0V trip.

NOTE

If both the high voltage mains supply and 24 Vdc auxiliary control master pod supply are lost a delay of approximately 3 minutes should be maintained to allow the DC bus to delay below 35 Vdc before reapplying the 24 Vdc control master supply to avoid a LV mode over voltage trip or ‘inh’ status display.

Figure 1-2 Location of DIN rail user terminals



1.1 User connections

With reference to the appropriate wiring diagrams Figure 1-3 *Unidrive SP6 wiring diagram* and Figure 1-4 *Unidrive SP7 wiring diagram* and Table 1-1 below, establish the following connections:

Table 1-1 Description of DIN rail user terminals

Terminal number	Description	Function	
1	User terminal	0 Vdc from external supply	Ensure the 24 Vdc supply is common to both the Control Master terminals (1 and 2) and DIN rail user terminals (1 and 2).
2	Fuse holder	+24 Vdc Fused by 6.3 A fast blow from external supply	
A2-	Timer relay	0 Vdc from external supply	

Figure 1-3 Unidrive SP6 wiring diagram

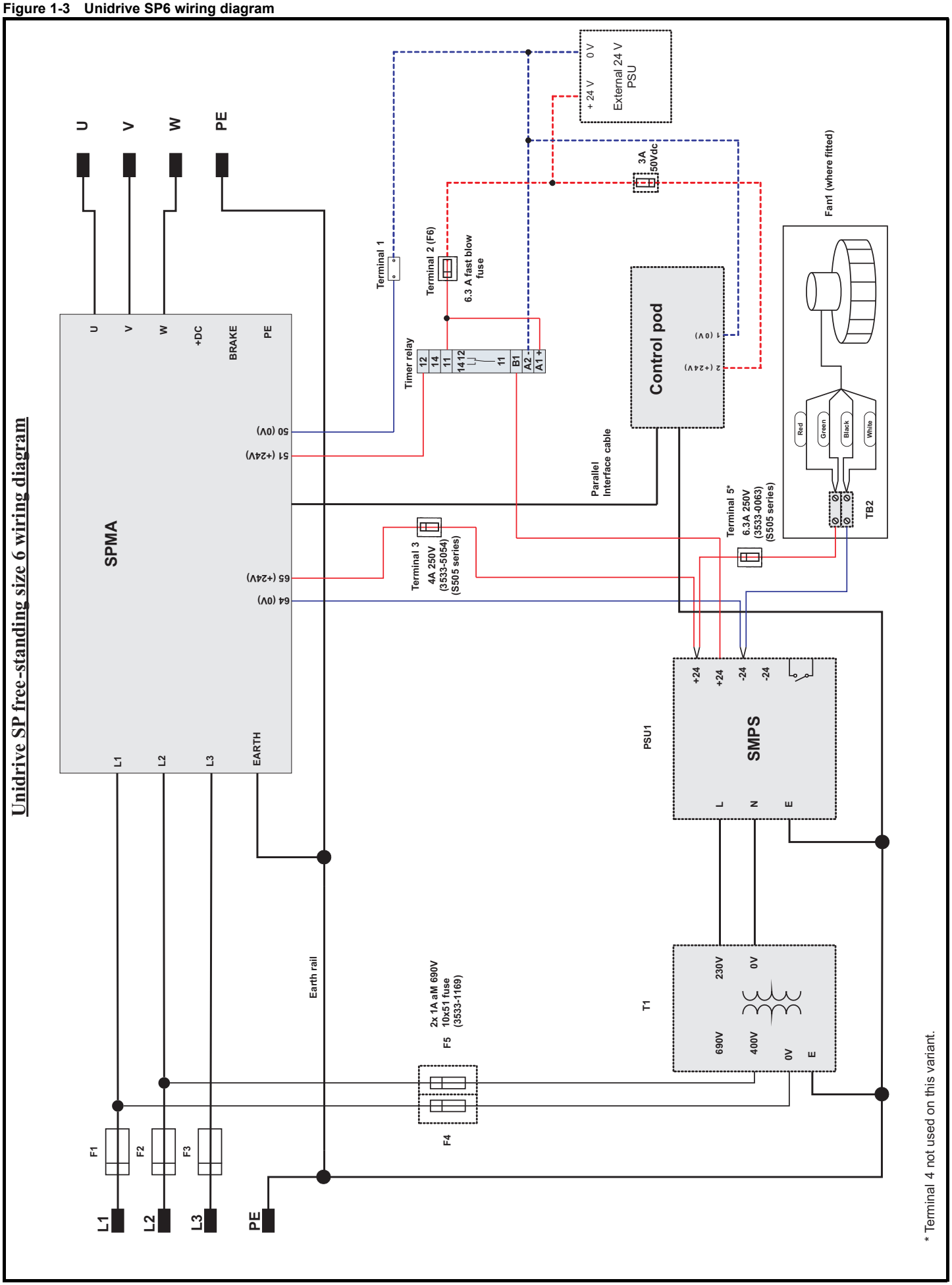


Figure 1-4 Unidrive SP7 wiring diagram